FIG. 1

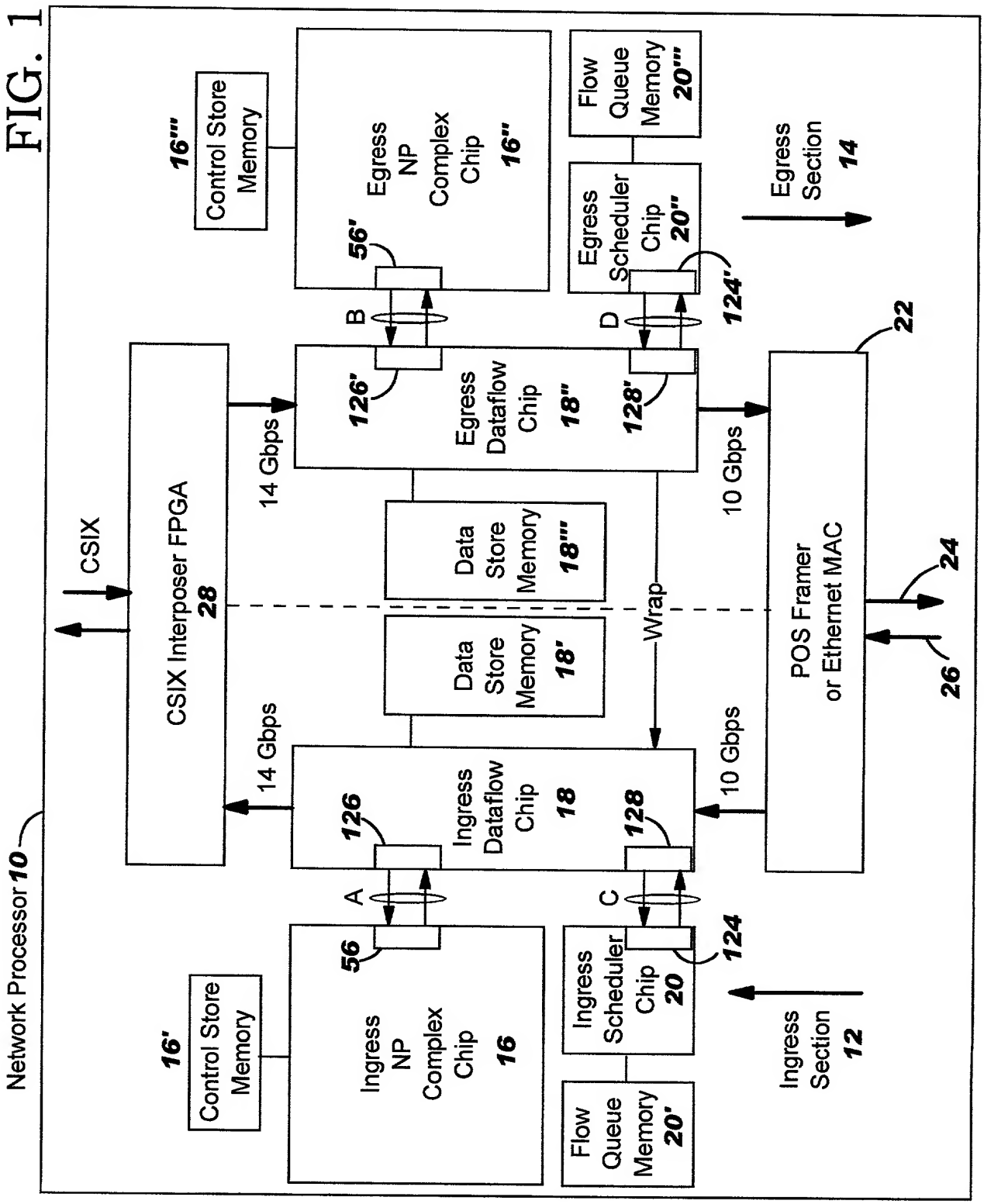

Network Processor 10
CSIX
CSIX Interposer FPGA 28
14 Gbps
14 Gbps
Ingress Dataflow Chip 18
126
128
Egress Dataflow Chip 18"
126'
128'
Data Store Memory 18'
Data Store Memory 18"
Wrap
10 Gbps
10 Gbps
POS Framer or Ethernet MAC
22
24
26
A
B
C
D
56
56'
124
124'
Ingress NP Complex Chip 16
Egress NP Complex Chip 16"
Ingress Scheduler Chip 20
Egress Scheduler Chip 20"
Control Store Memory 16'
Control Store Memory 16"
Flow Queue Memory 20'
Flow Queue Memory 20"
Ingress Section 12
Egress Section 14

FIG. 2

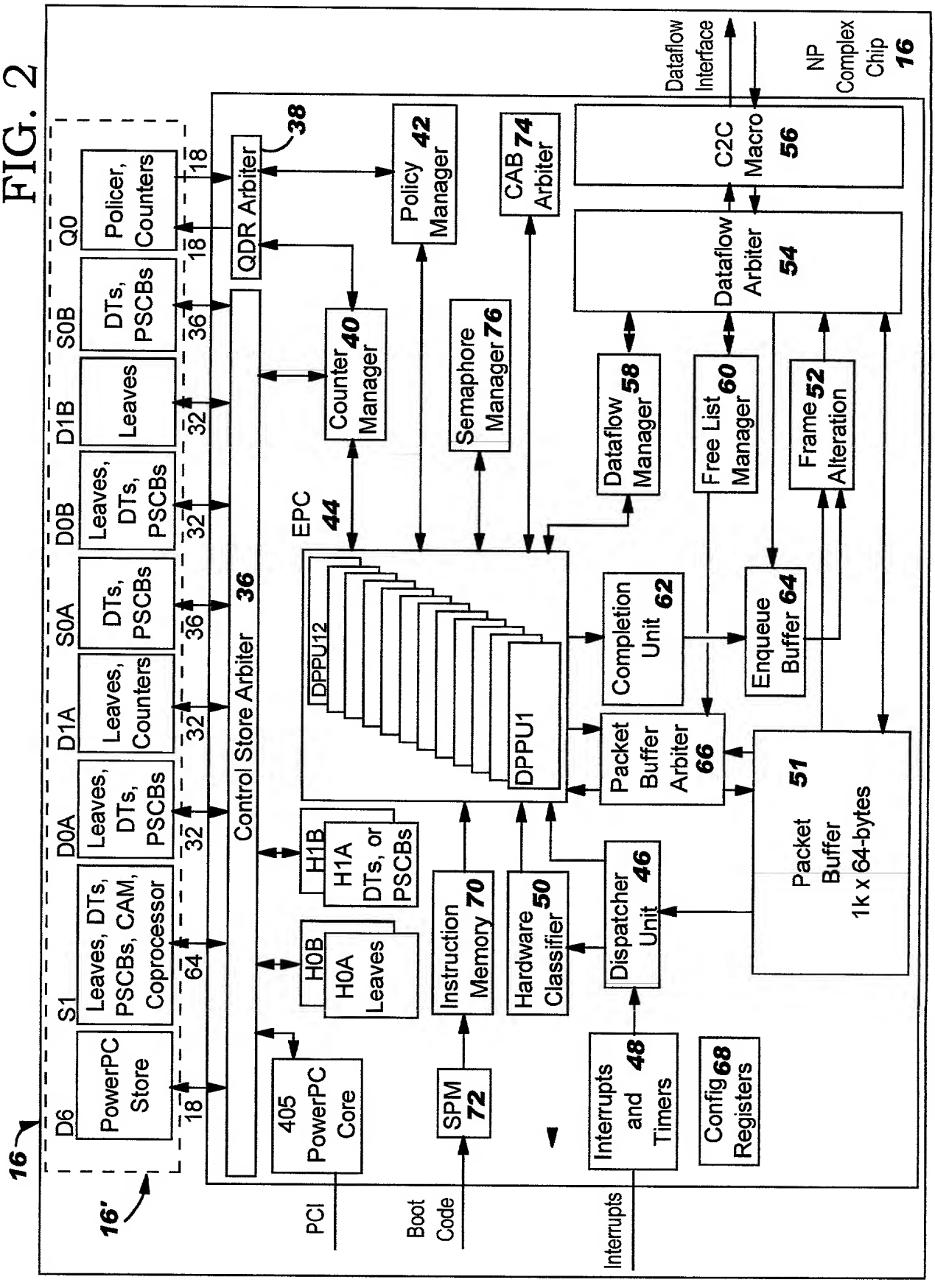

16
16'
D6
PowerPC Store
18
S1
Leaves, DTs, PSCBs, CAM, Coprocessor
64
D0A
Leaves, DTs, PSCBs
32
D1A
Leaves, Counters
32
S0A
DTs, PSCBs
36
D0B
Leaves, DTs, PSCBs
32
D1B
Leaves
32
S0B
DTs, PSCBs
36
Q0
Policer, Counters
18
18
Control Store Arbiter 36
QDR Arbiter 38
Policy 42 Manager
CAB 74 Arbiter
Counter 40 Manager
Semaphore Manager 76
EPC 44
DPPU12
DPPU1
Dataflow 58 Manager
Free List 60 Manager
Frame 52 Alignment
C2C Macro 56
Dataflow Arbiter 54
Dataflow Interface
NP Complex Chip 16
Completion Unit 62
Enqueue Buffer 64
Packet Buffer Arbiter 66
Packet 51 Buffer 1k x 64-bytes
H1B
H1A DTs, or PSCBs
H0B
H0A Leaves
Instruction Memory 70
Hardware 50 Classifier
Dispatcher 46 Unit
405 PowerPC Core
SPM 72
Interrupts and 48 Timers
Config 68 Registers
PCI
Boot Code
Interrupts

FIG. 3

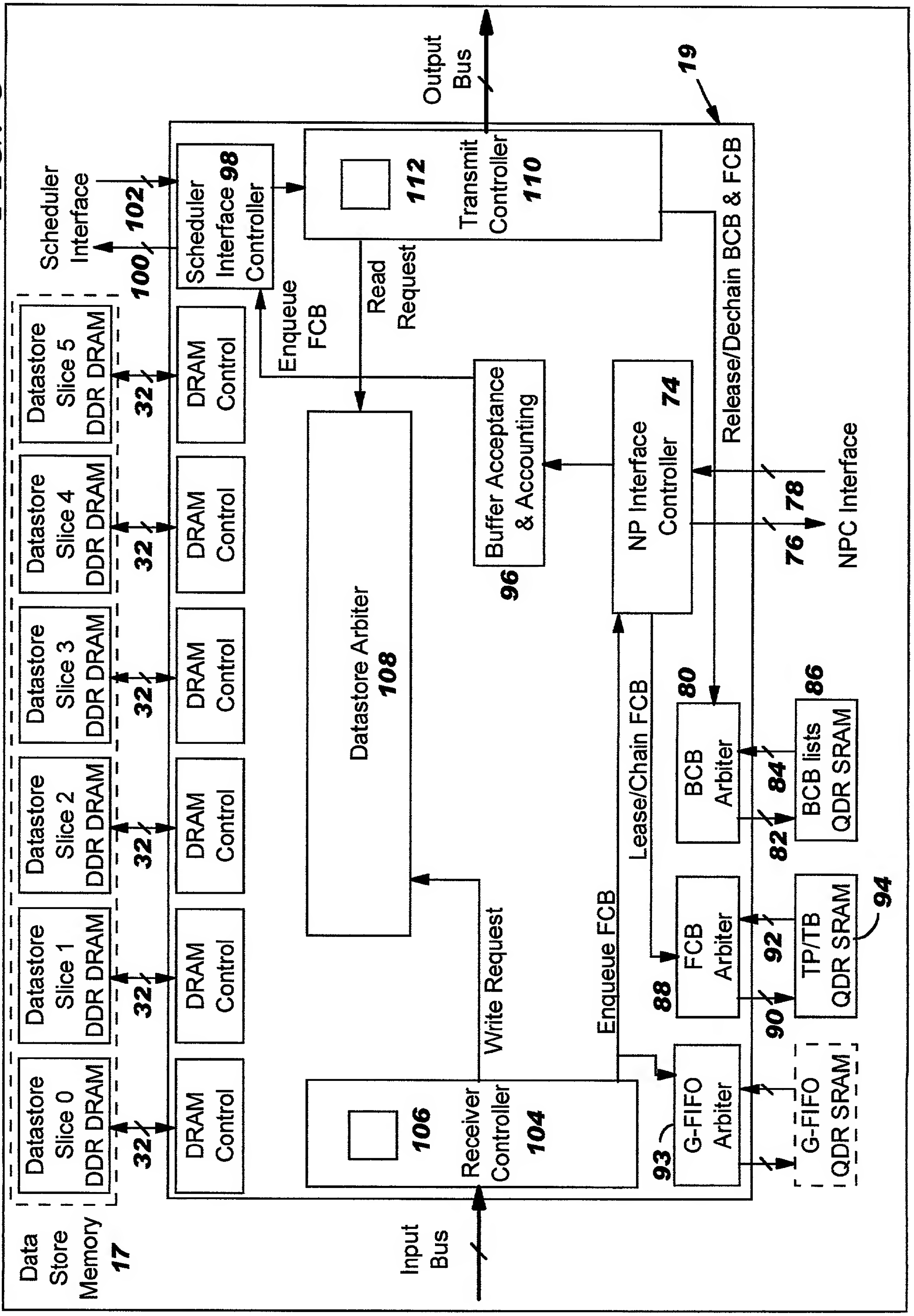

Data Store Memory 17
Datastore Slice 0 DDR DRAM
Datastore Slice 1 DDR DRAM
Datastore Slice 2 DDR DRAM
Datastore Slice 3 DDR DRAM
Datastore Slice 4 DDR DRAM
Datastore Slice 5 DDR DRAM
32
DRAM Control
Scheduler Interface
100
102
Scheduler Interface 98 Controller
Output Bus
19
Transmit Controller 110
112
Read Request
Enqueue FCB
Datastore Arbiter 108
Buffer Acceptance & Accounting
96
NP Interface Controller 74
Release/Dechain BCB & FCB
76
78
NPC Interface
Write Request
Lease/Chain FCB
Enqueue FCB
BCB Arbiter
80
82
84
BCB lists QDR SRAM
86
FCB Arbiter
88
90
92
TP/TB QDR SRAM
94
G-FIFO Arbiter
93
G-FIFO QDR SRAM
Receiver Controller 104
106
Input Bus

FIG. 4

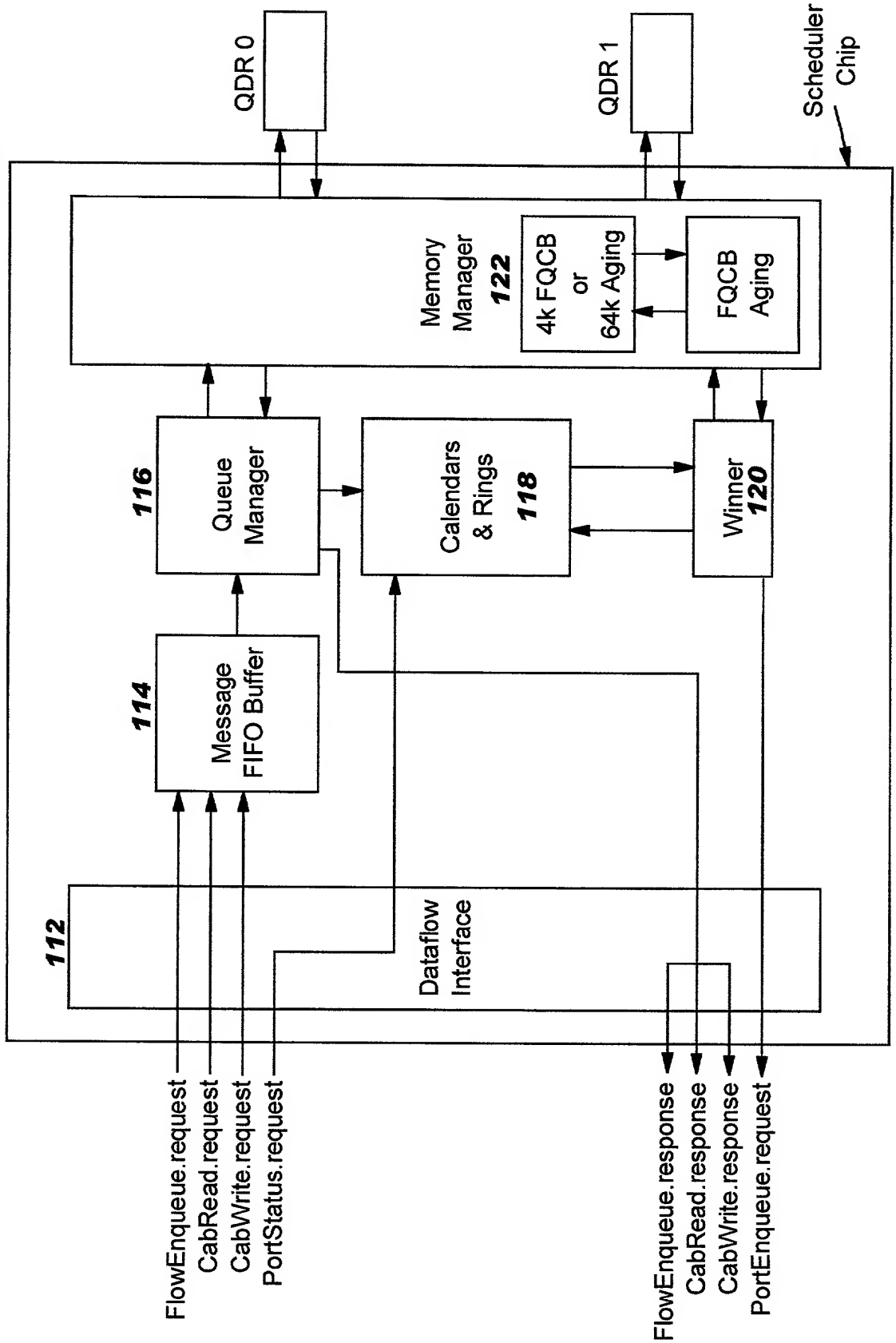

QDR 0
QDR 1
Scheduler Chip
Memory Manager 122
4k FQCB or 64k Aging
FQCB Aging
116
Queue Manager
Calendars & Rings 118
Winner 120
114
Message FIFO Buffer
112
Dataflow Interface
FlowEnqueue.request
CabRead.request
CabWrite.request
PortStatus.request
FlowEnqueue.response
CabRead.response
CabWrite.response
PortEnqueue.request

FIG. 5

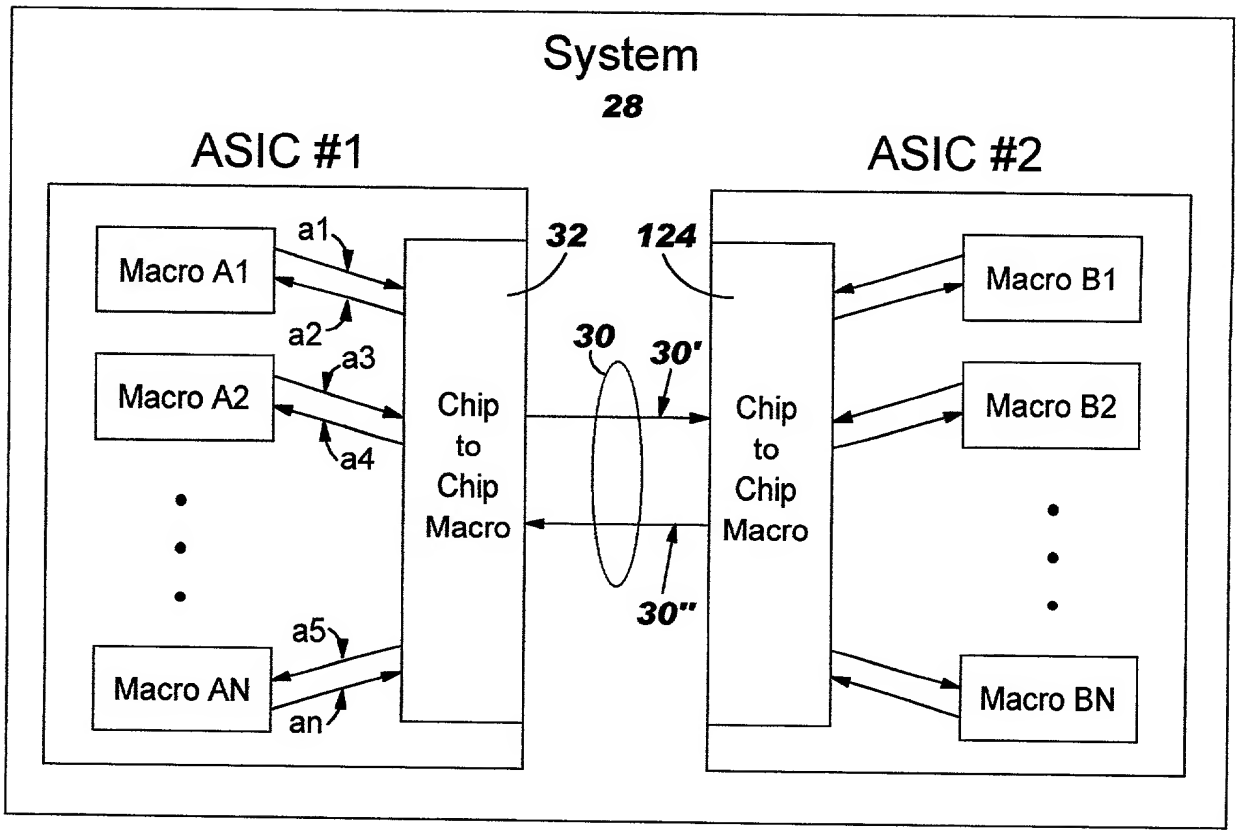

System
28
ASIC #1
ASIC #2
Macro A1
Macro A2
Macro AN
a1
a2
a3
a4
a5
an
32
124
30
30'
30"
Chip to Chip Macro
Chip to Chip Macro
Macro B1
Macro B2
Macro BN

FIG. 5A

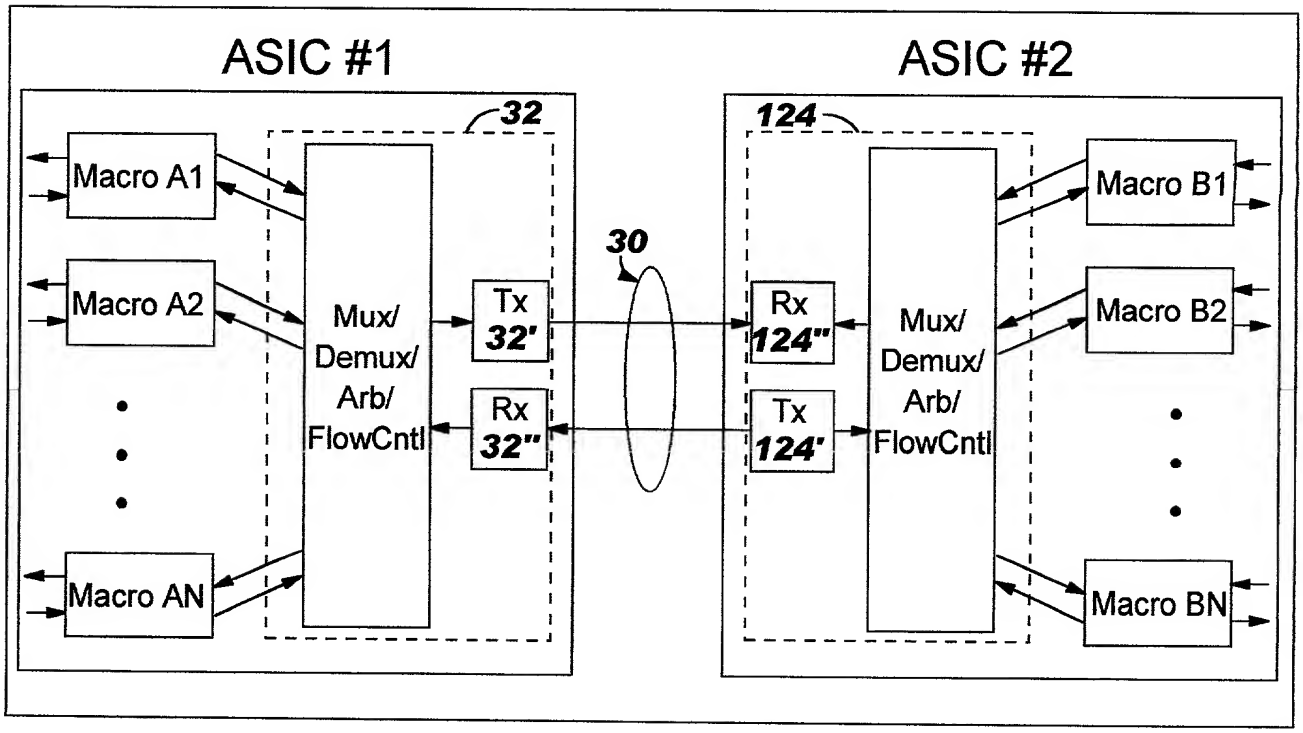

ASIC #1
ASIC #2
32
124
30
Macro A1
Macro A2
Macro AN
Mux/
Demux/
Arb/
FlowCntl
Tx
32'
Rx
32"
Rx
124"
Tx
124'
Mux/
Demux/
Arb/
FlowCntl
Macro B1
Macro B2
Macro BN

FIG. 6

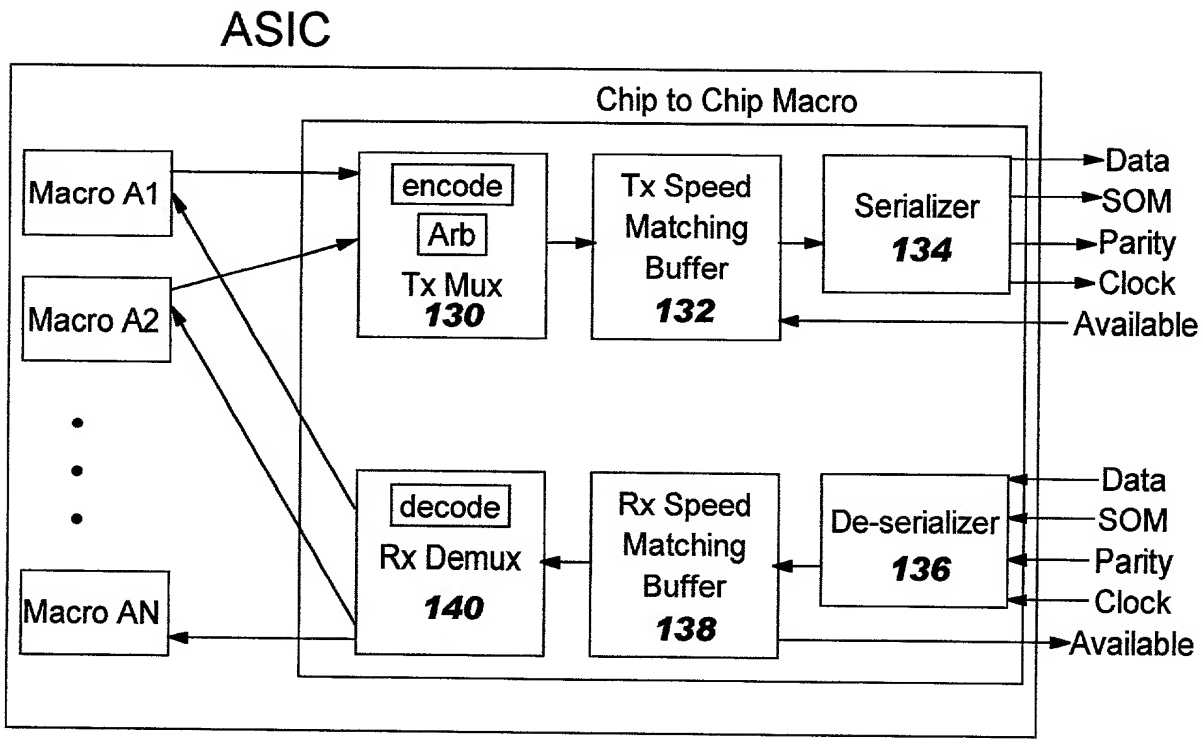

ASIC
Chip to Chip Macro
Macro A1
Macro A2
Macro AN
encode
Arb
Tx Mux
130
Tx Speed
Matching
Buffer
132
Serializer
134
Data
SOM
Parity
Clock
Available
decode
Rx Demux
140
Rx Speed
Matching
Buffer
138
De-serializer
136
Data
SOM
Parity
Clock
Available

FIG. 7

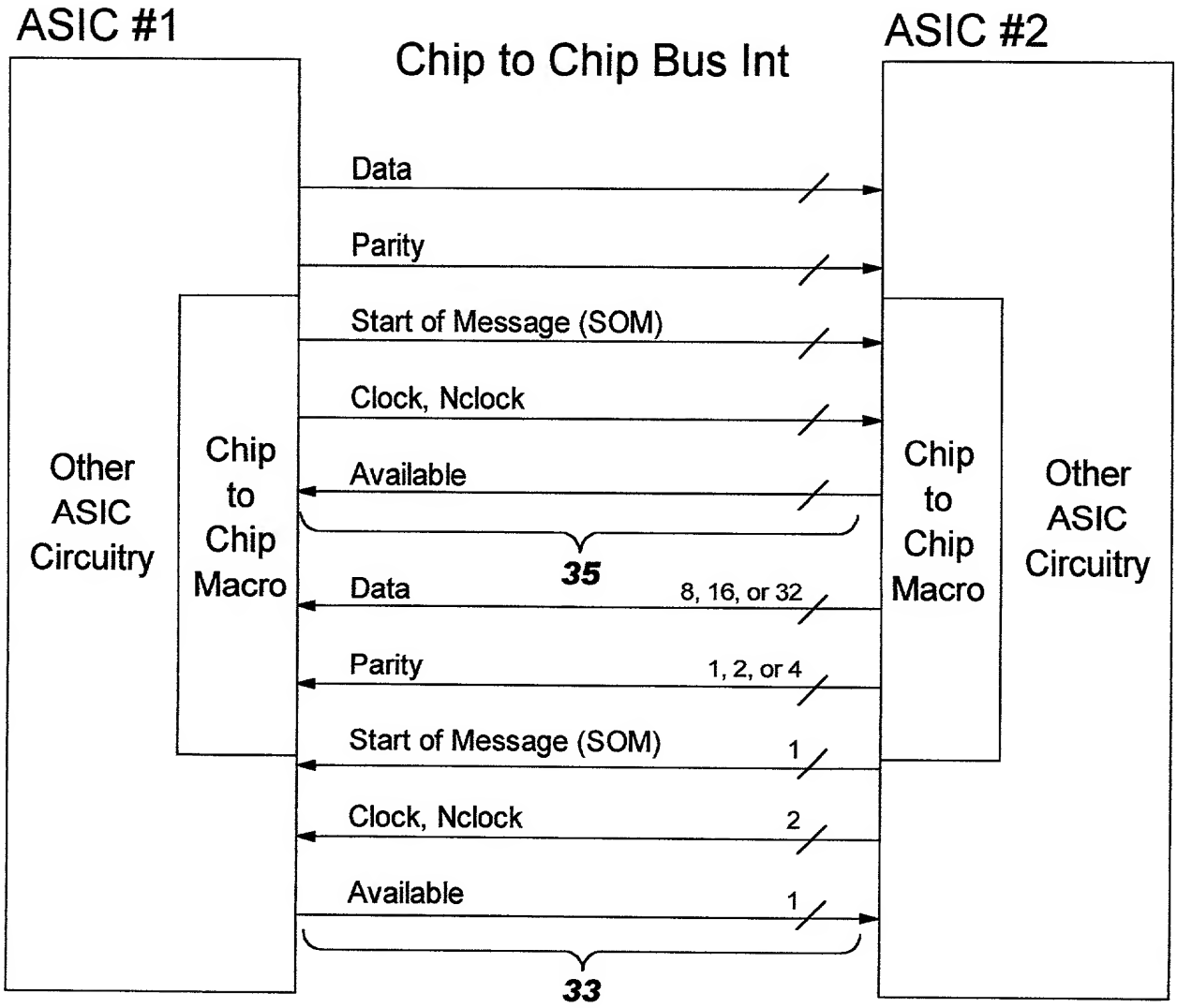

ASIC #1
Chip to Chip Bus Int
ASIC #2
Data
Parity
Start of Message (SOM)
Clock, Nclock
Available
Other ASIC Circuitry
Chip to Chip Macro
Chip to Chip Macro
Other ASIC Circuitry
35
Data
8, 16, or 32
Parity
1, 2, or 4
Start of Message (SOM)
1
Clock, Nclock
2
Available
1
33

FIG. 8

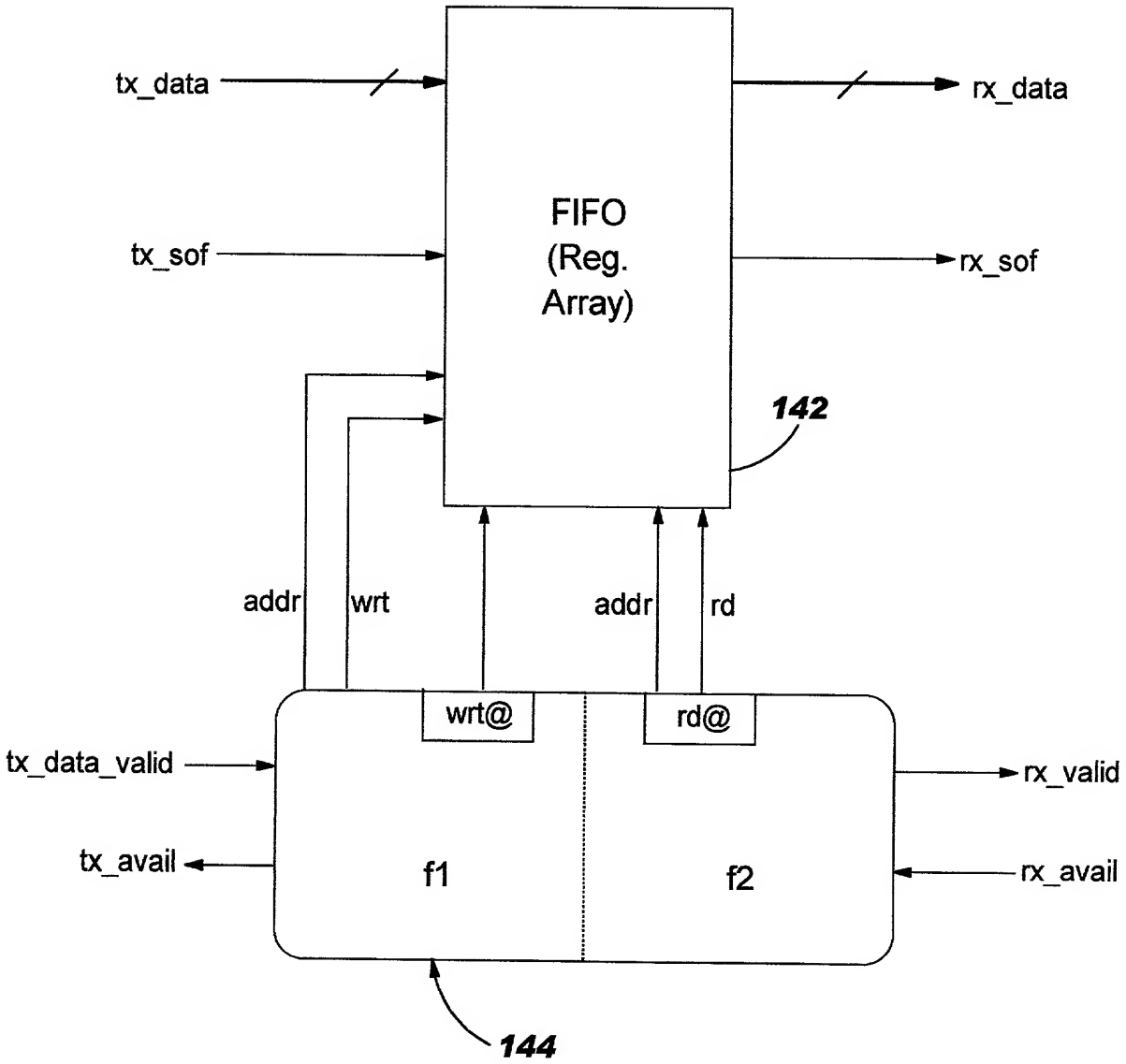
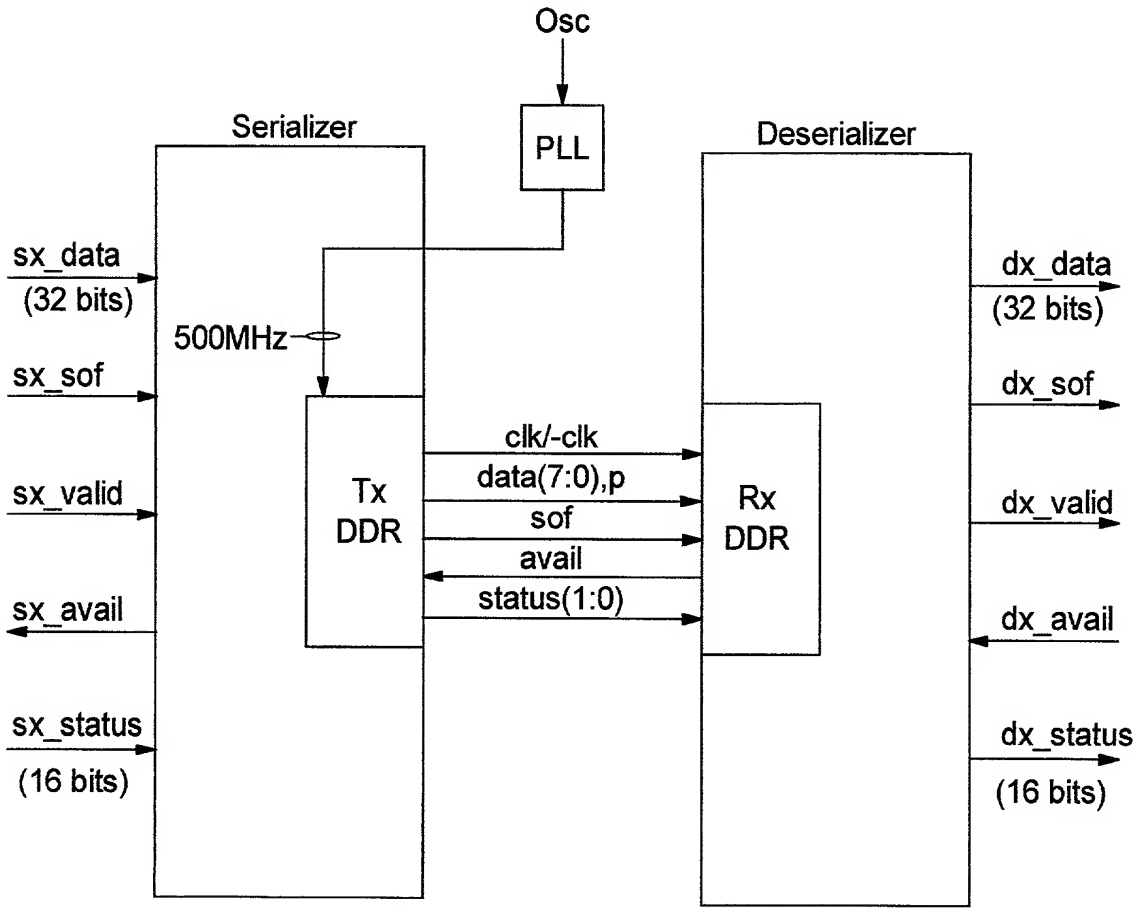

tx_data
rx_data
FIFO
(Reg.
Array)
tx_sof
rx_sof
142
addr
wrt
addr
rd
wrt@
rd@
tx_data_valid
rx_valid
tx_avail
f1
f2
rx_avail
144

FIG. 9


Osc
PLL
Serializer
Deserializer
sx_data
(32 bits)
500MHz
sx_sof
sx_valid
sx_avail
sx_status
(16 bits)
Tx
DDR
clk/-clk
data(7:0),p
sof
avail
status(1:0)
Rx
DDR
dx_data
(32 bits)
dx_sof
dx_valid
dx_avail
dx_status
(16 bits)